8-bit x 3 Serial-In/Parallel-Out Constant Current Driver

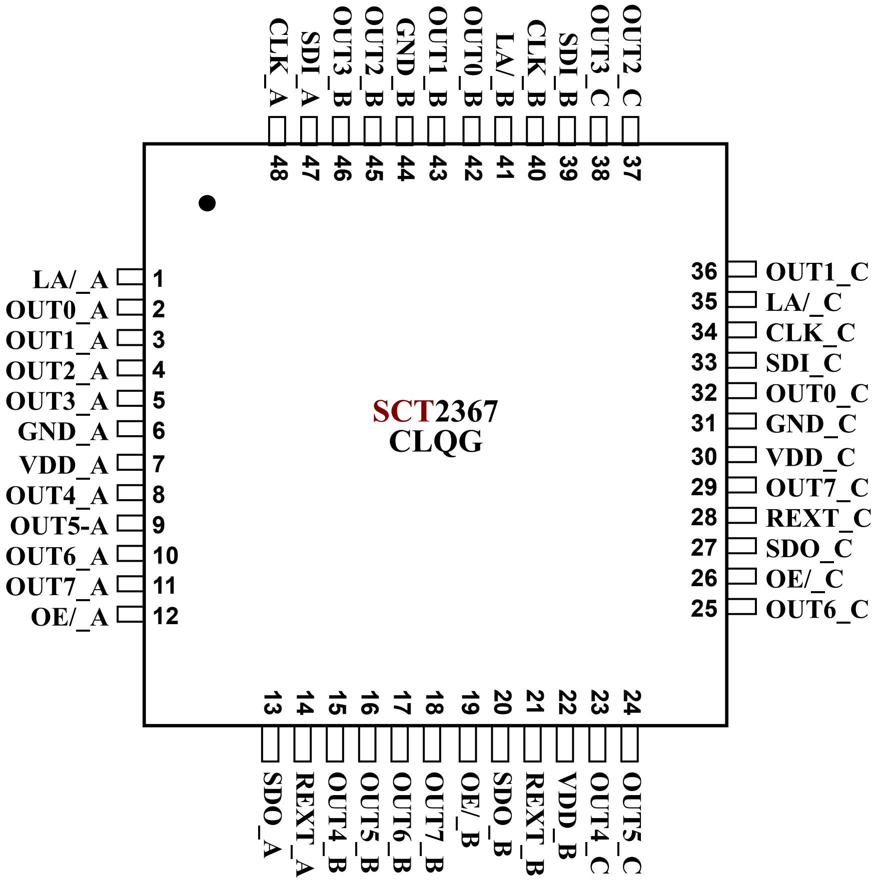
Product Description

The SCT2367 serial-interfaced LED driver sinks 24 LED clusters with constant current to keep uniform intensity of LED displays. In applications, three external resistors are used to set the full-scale constant output current from 5mA up to 45mA. The SCT2367 guarantees each output can endure maximum 17V DC stress. The built-in shift registers and data latches making the SCT2367 an effective solution in driving LED display. The SCT2367 incorporate three 8-channel drivers, and users can adjust output current through three external resistors. The output enable function with 3 output enable pins gates 24 outputs on and off, and is fast enough to be used as PWM input for LED intensity control. Since the serial data input rate can be reached up to 25MHz, the SCT2367 will satisfy a system which needs high volume data transmission to control the LED display.

Features

- 24 constant current sinker with LED power-supply voltage up to 17V
- Constant output current : 5-45mA@5V , 5-30mA@3.3V
- Excellent current regulation to load, supply voltage and temperature
- ±2% current matching between outputs
- ±3% current matching between ICs
- Fast output current control: Minimum PWM pulse width = 180ns
- Output current are programmed using three external resistors
- CMOS Schmitt trigger inputs with clock rate up to 25MHz
- Operating supply voltage range of 3.3V to 5.5V
- Built-in power on reset circuit forces all the outputs off while power on
- Interlaced 30nS delay between outputs to reduce the bouncing noise
- Package: LQFP48
- Applications: LED Displays, Variable Message Signs, LED Traffic Signs

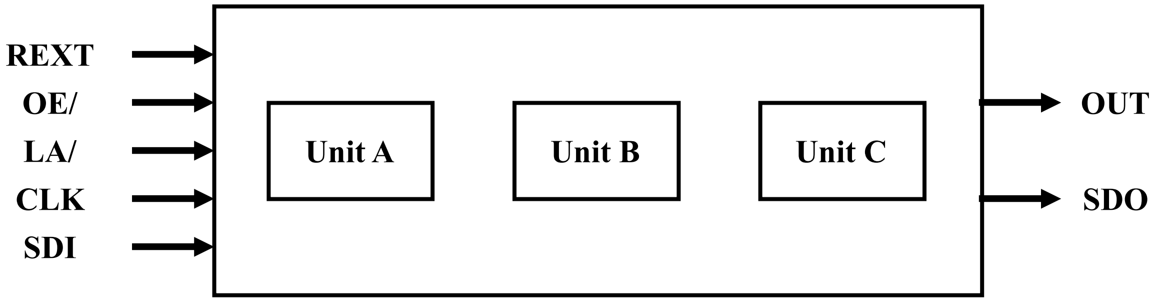
Pin Configurations



Terminal Description

Pin Name	Block Pin No.			Function
	A	B	C	
GND	6	44	31	Ground terminal
SDI	47	39	33	Serial input of data shift register.
CLK	48	40	34	Clock input of shift register, data is sampled at the rising edge of CLK.
LA/	1	41	35	Input terminal of data strobe. Data is latched when LA/ is low. And data on shift register goes through when LA/ is high
OUT[0:7]	2, 3, 4, 5, 8, 9, 10,11,	42,43, 45,46, 15,16, 17,18,	32,36, 37,38, 23,24, 25,29,	Open-drain, constant-current outputs.
OE/	12	19	26	Output enable signal. Output is enabled when OE/ is forced to low.
SDO	13	20	27	Output terminal of serial-data output to the SDI of next SCT2367.
REXT	14	21	28	Used to connect an external resistor for setting up all output current
VDD	7	22	30	Supply voltage terminal

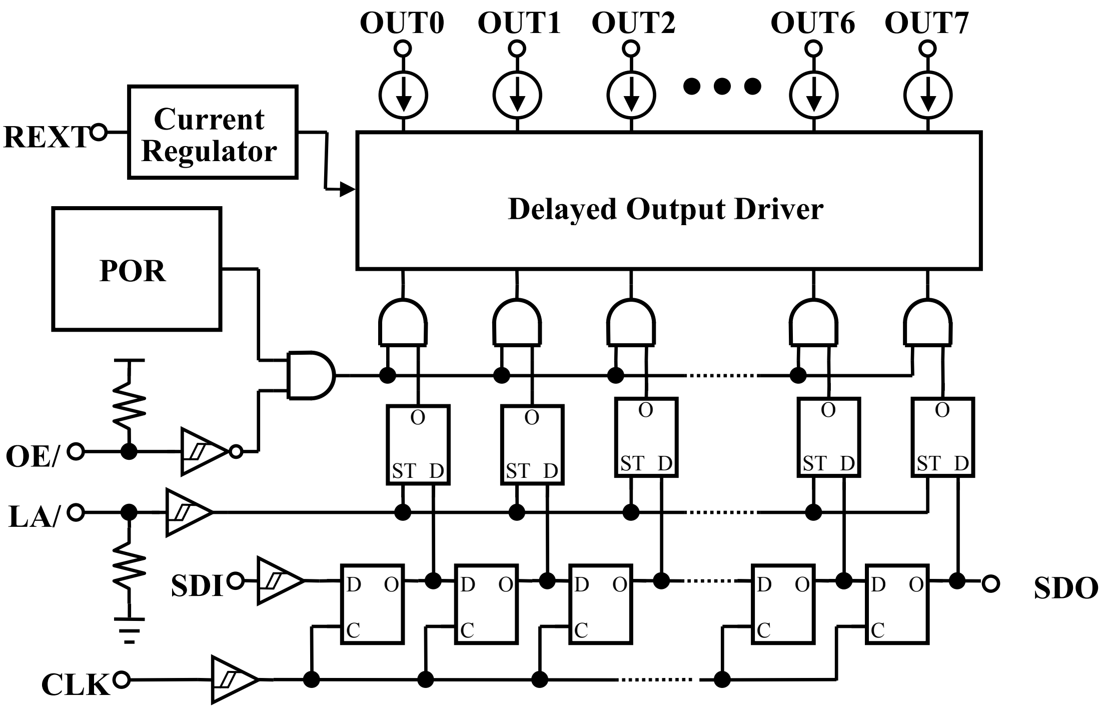
Block Diagram



SCT2367

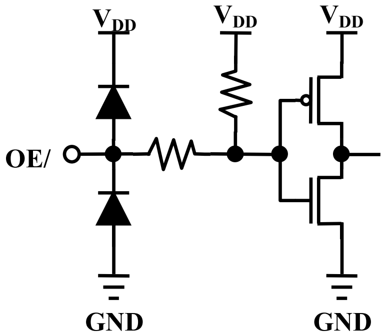
1. SCT2367 contains three 8-channel constant current drivers in one package, named “Unit A”,”Unit B”, “Unit C”. As shown in Pin Configuration, pins are divided into three groups, A, B,C. Pin Names are not limited to one specific group in the rest of the content, but all the information will be applied to the three groups.
2. The block diagram of each basic unit is shown as below,

Block Basic Unit

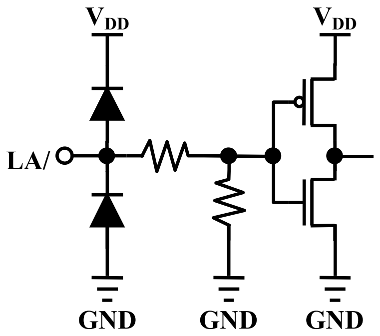


SCT2367

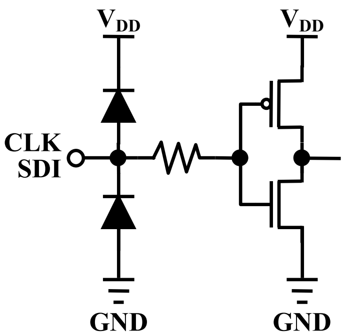
Equivalent Circuits of Inputs (1)



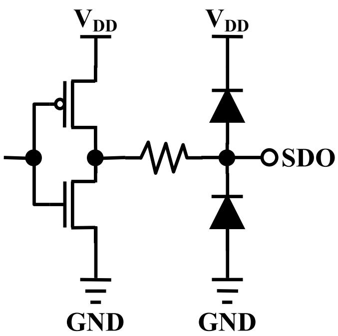
Equivalent Circuits of Input (2)



Equivalent Circuits of Inputs (3)



Equivalent Circuits of Output



Ordering Information

Part	Marking	Package	Unit per reel(pcs)
SCT2367CLQG	SCT2367CLQG	Green LQFP48L 7*7mm	N/A

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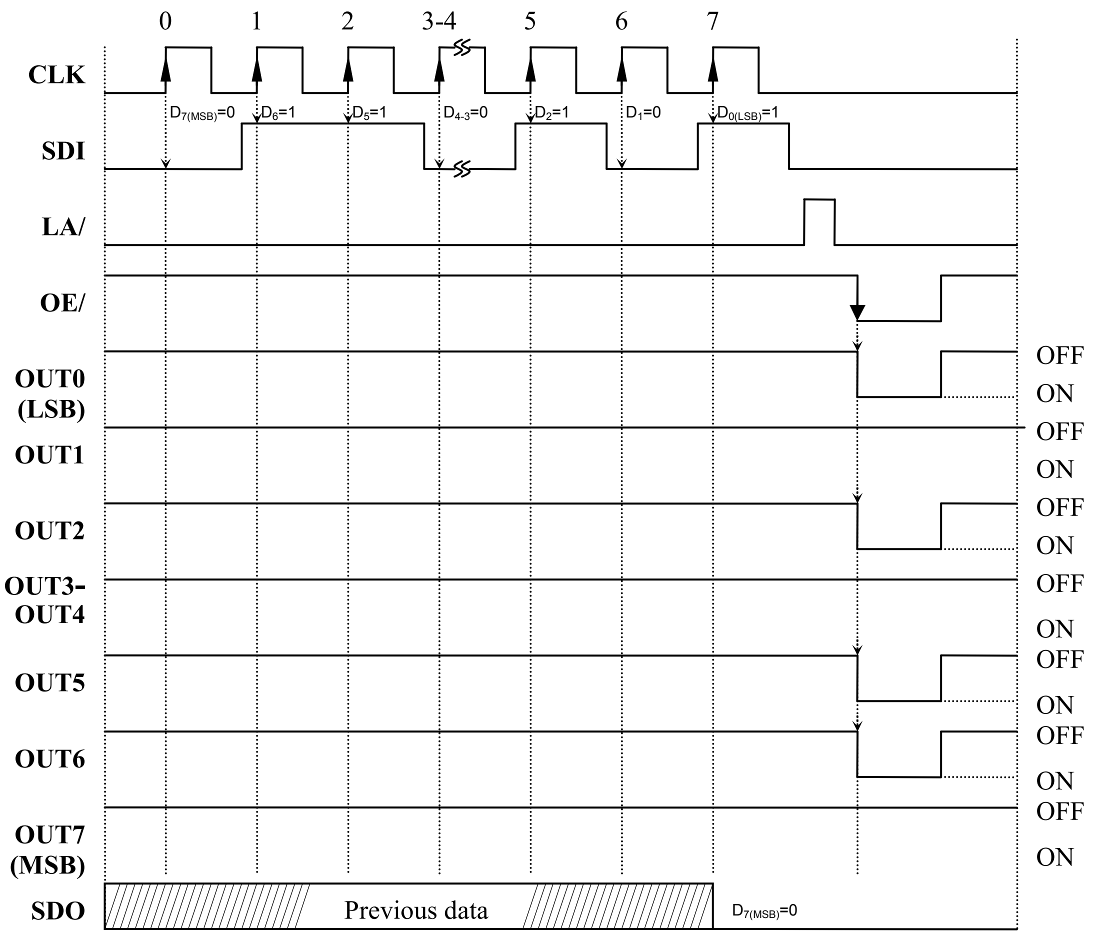
E-mail : service@starchips.com.tw

Truth Table

CLK	LA/	OE/	SDI	OUT0 ~ OUT7	SDO
↑	H	L	D_n	D_n D_{n-1} ---- D_{n-6} D_{n-7}	D_{n-7}
↑	L	L	D_{n+1}	No change	D_{n-6}
↑	H	L	D_{n+2}	D_{n+2} D_{n+1} ---- D_{n-4} D_{n-5}	D_{n-5}
↓	X	L	D_{n+3}	D_{n+2} D_{n+1} ---- D_{n-4} D_{n-5}	D_{n-5}
↓	X	H	D_{n+3}	Off	D_{n-5}

Timing Diagram



Maximum Ratings (T_A = 25°C)

Characteristic	Symbol	Rating	Unit
Supply voltage	V_{DD}	7.0	V
Input voltage	V_{IN}	-0.2 ~ V_{DD}+0.2	V
Output current	I_{OUT}	60	mA/Channel
Output voltage	V_{OUT}	-0.2 ~ 17.0	V
Total GND terminal current for each unit	I_{GND}	480	mA
Power Dissipation(on PCB)	P_{DI}	2.38	W
Thermal Resistance(on PCB)	$R_{TH(j-a)I}$	52.6	°C /W
Operating temperature	T_{OPR}	-40~+85	°C
Storage temperature	T_{STG}	-55~+150	°C

The absolute maximum ratings are a set of ratings not to be exceeded. Stresses beyond those listed under "Maximum Ratings" may cause the device breakdown, deterioration even permanent damage. Exposure to the maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_A= -40 to 85°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-	3	-	5.5	V
Output voltage	V_{OUT}	Output OFF	-	-	17	V
		Output ON	-	1[1]	4[2]	V
Output current	I_{OUT}	V_{DD}=3.3/5V, V_{OUT}=1V	5	-	30/45	mA
Input voltage	V_{IH}	input signals	0.7V_{DD}	-	V_{DD}	V
	V_{IL}		0	-	0.3V_{DD}	V
OE/ pulse width	$t_{W(OE)}$	V_{DD}=3.3V/5V	180	-	-	ns

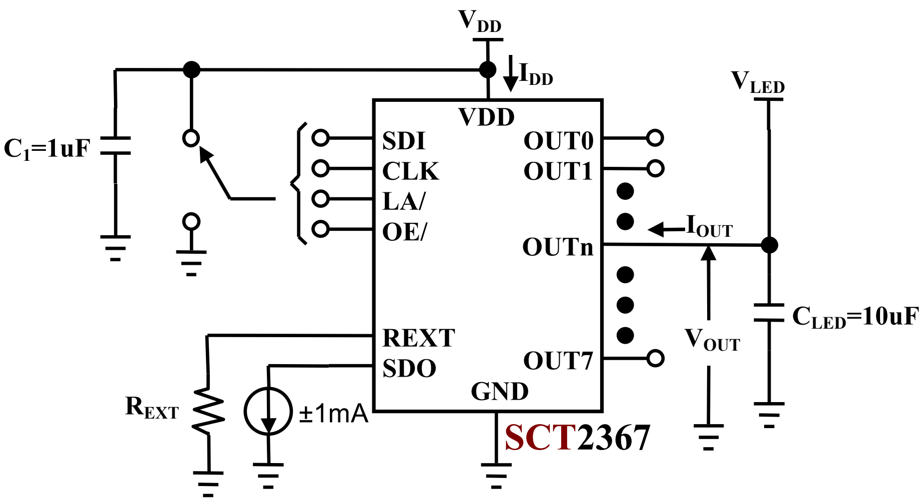
1. The output current keep constant in range of 5-45mA if V_{OUT}=1V.
   However, user can minimize V_{OUT} to reduce power dissipation according to used current, e.g., set V_{OUT} to 0.6V if I_{OUT}=20mA.
2. The maximum Vout is package thermal limited, user should keep Vout under maximum power dissipation.

Electrical Characteristics (V_{DD}=3.3/5V, T_A=25°C unless otherwise noted)

Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Digital inputs voltage		V_{IH}	-	0.7V_{DD}	-	V_{DD}	V
		V_{IL}	-	0	-	0.3V_{DD}	V
SDO output voltage		V_{OH}	V_{DD}=3.3/5V, I_{OH}= -1mA	V_{DD}-0.4	-	-	V
		V_{OL}	V_{DD}=3.3/5V, I_{OL}= +1mA	-	-	0.4	V
Output leakage current		I_{OL}	V_{OUT}=17V	-	-	0.5	uA
Output current		I_{OUT}	V_{OUT}=1V, R_{EXT}=900Ω	-	21	-	mA
Current bit skew[1]		dI_{OUT1}	V_{OUT}=1V, R_{EXT}=900Ω	-	±2	±3	%
Chip skew[2]		dI_{OUT2}	V_{OUT}=1V, R_{EXT}=900Ω	-	±3	±6	%
Line regulation[3] I_{OUT} vs. V_{DD}		%/dV_{DD}	3V<V_{DD}<5.5V, V_{OUT}>1V, R_{EXT}=900Ω	-	±0.5	±1	%/V
Load regulation[4] I_{OUT} vs. V_{OUT}		%/dV_{OUT}	1V<V_{OUT}<4V, I_{OUT}=42mA, R_{EXT}=900Ω	-	±0.1	±0.5	%/V
Temp. regulation[5] I_{OUT} vs. T_A		%/dT_A	-20°C < T_A < 80°C, I_{OUT}=10mA~90mA,V_{DD}=5V	-	±0.005	-	%/°C
Pull-up resistor		R_{UP}	OE/	-	420	-	KΩ
Pull-down resistor		R_{DOWN}	LA/	-	400	-	KΩ
Supply current	OFF	$I_{DD(OFF)1}$	V_{DD}=3.3/5V, R_{EXT}=Open, OUT[0:7]=OFF	-	2	3	mA
		$I_{DD(OFF)2}$	V_{DD}=3.3/5V, R_{EXT}=900Ω, OUT[0:7]=OFF	-	5	7	
	ON	$I_{DD(ON)}$	V_{DD}=3.3/5V, R_{EXT}=900 Ω, OUT[0:7]=ON	-	7/8	10	

1. Bit skew=(I_{OUT}-I_{AVG}) / I_{AVG}, where I_{AVG}=($I_{OUT(max)}$+ $I_{OUT(min)}$)/2
2. Chip skew=(I_{AVG}-I_{CEN}) / I_{CEN}*100(%), where I_{CEN} is the statistics distribution center of output currents.
3. Line regulation=[I_{OUT}(V_{DD}=5.5V)-I_{OUT}(V_{DD}=3V)] / {[I_{OUT}(V_{DD}=5.5V)+I_{OUT}(V_{DD}=3V)]/2} / (5.5V-3V)*100(%/V)
4. Load regulation=[I_{OUT}(V_{OUT}=4V)-I_{OUT}(V_{OUT}=1V)] / {[I_{OUT}(V_{OUT}=4V)+I_{OUT}(V_{OUT}=1V)]/2} / (4V-1V)*100(%/V)
5. Temperature regulation=[I_{OUT}(T_A=80°C)-I_{OUT}(T_A=-20°C)] / {[I_{OUT}(T_A=80°C)+I_{OUT}(T_A=-20°C)]/2} / (80°C+20°C)*100(%/°C)

Test Circuit for Electrical Characteristics



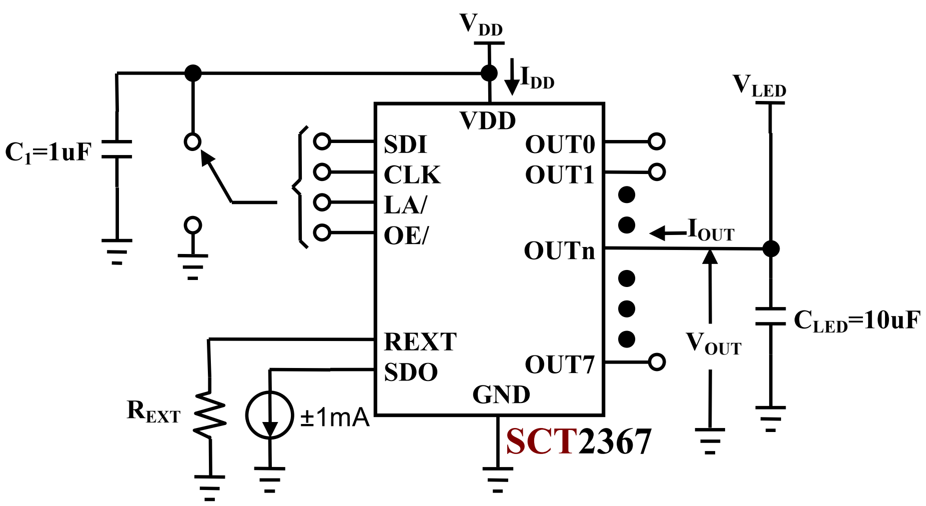
Place C_1/C_{LED} as close to IC VDD/OUT pin(not supply source) as possible.

Switching Characteristics (T_A=25°C unless otherwise noted)

Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time ("L" to "H")	CLK - OUTn	t_{PLH1}	V_{DD} = 3.3/5V V_{LED} = 5V V_{IH} = V_{DD} V_{IL}= GND R_{EXT} = 900Ω R_L = 180Ω C_L = 10pF C_1 = 1uF C_{LED} = 10uF	-	80	100	ns
	LA/ - OUTn	t_{PLH2}		-	80	100	ns
	OE/ - OUT0	t_{PLH3}		-	80	100	ns
	CLK - SDO	t_{PLH}		-	20	40	ns
Propagation delay time ("H" to "L")	CLK - OUTn	t_{PHL1}		-	80	100	ns
	LA/ - OUTn	t_{PHL2}		-	80	100	ns
	OE/ - OUT0	t_{PHL3}		-	80	100	ns
	CLK - SDO	t_{PHL}		-	20	40	ns
Pulse width	CLK	$t_{W(CLK)}$		20	-	-	ns
	LA/	$t_{W(L)}$		20	-	-	ns
	OE/	$t_{W(OE)}$		180	-	-	ns
Setup time for SDI		$t_{S(D)}$		5	-	-	ns
Hold time for SDI		$t_{HD)}$		15			ns
Setup time for LA/		$t_{S(L)}$		5	-	-	ns
Hold time for LA/		$t_{H(L)}$		5	-	-	ns
SDO rise time		t_{SDOR}		-	20	-	ns
SDO fall time		t_{SDOF}		-	20	-	ns
Output rise time of I_{OUT}		t_{OR}		-	80	100	ns
Output fall time of I_{OUT}		t_{OF}		-	80	100	ns
Delayed output		t_{DR}	OUT_{EVEN} to OUT_{ODD}	-	30	-	ns
		t_{DF}		-	30	-	ns
Slow CLK rise time[1]		t_R	Cascade	-	-	500	ns
Slow CLK fall time		t_F		-	-	500	ns

1. It may not be possible to achieve the timing requirment for data transfer if t_R and t_F is too large during cascaded operation.

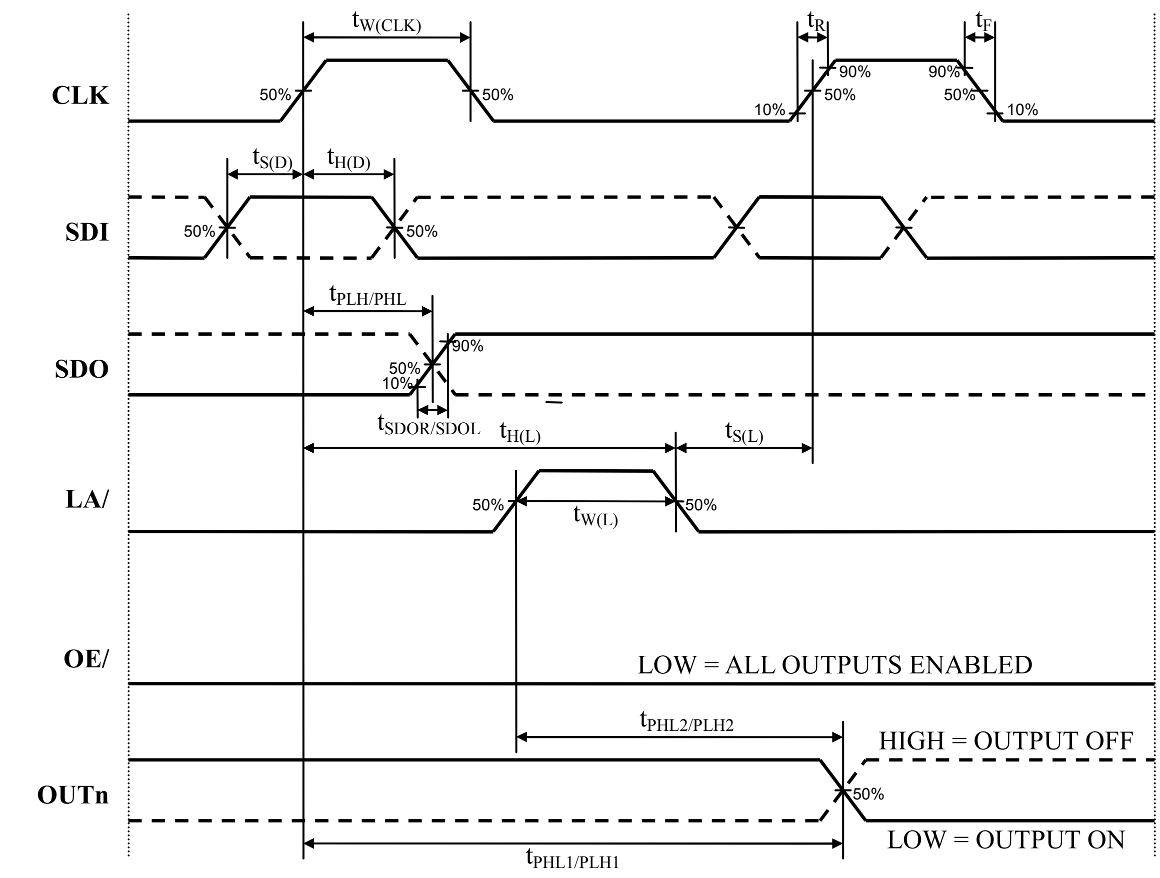
Test Circuit for Switching Characteristics



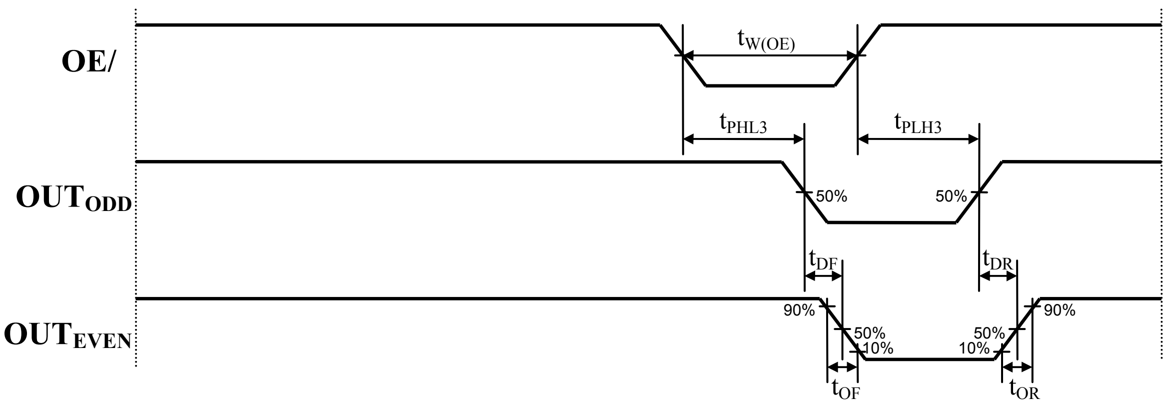
**Place C_1/C_{LED} as close to IC VDD/OUT pin(not supply source) as possible.*

Timing Waveform

LA/ Control Output

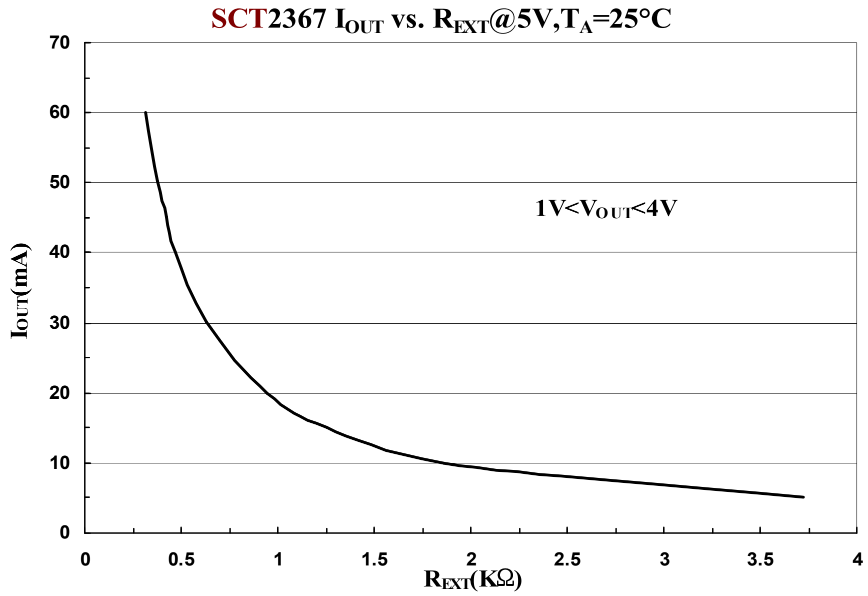


OE/ Control Output



Adjusting Output Current

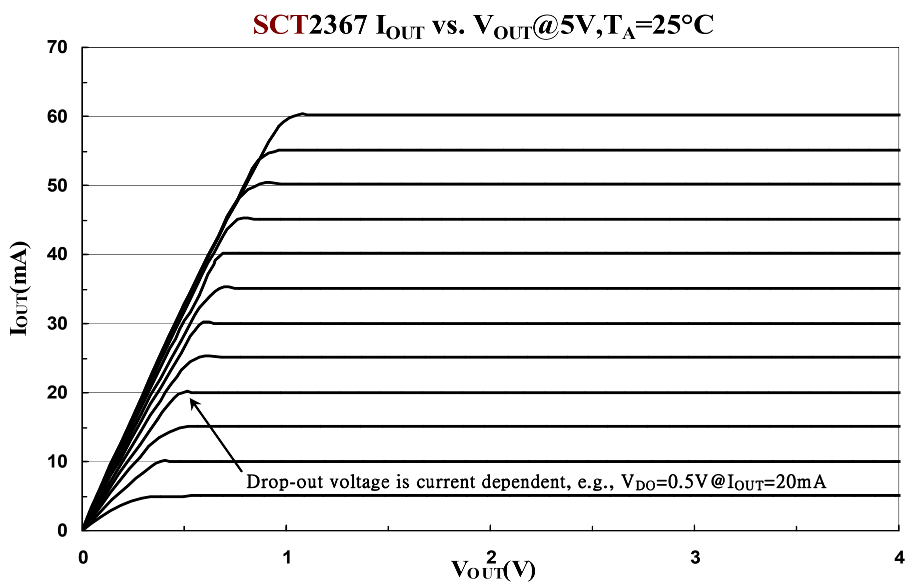
The SCT2367's output current (I_{OUT}) are set by one external resistor at pin REXT. The output current I_{OUT} versus resistance of R_{EXT} is shown as the following figure.

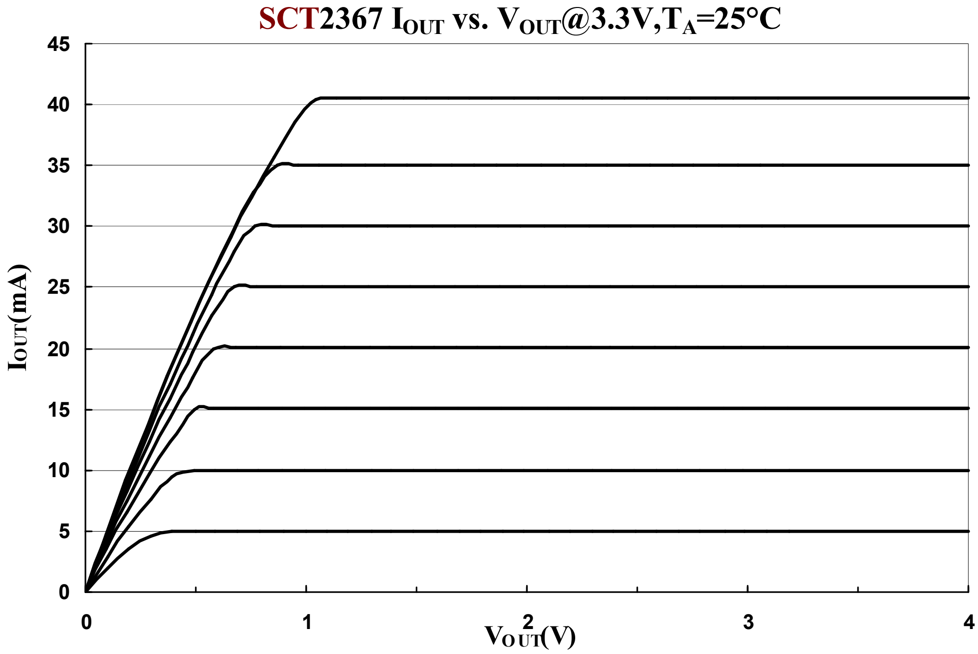


According to SCT2367' I-V curve, the output voltage should be larger than 1V to get 45 mA constant current. By applying proper output voltage, the SCT2367' output current set by an external resistor is approximate to: I_{OUT} = 30(630 / REXT) (mA) (chip skew < ±6%). Thus the output current is set to be about 21mA at REXT = 900Ω.

Output Characteristics

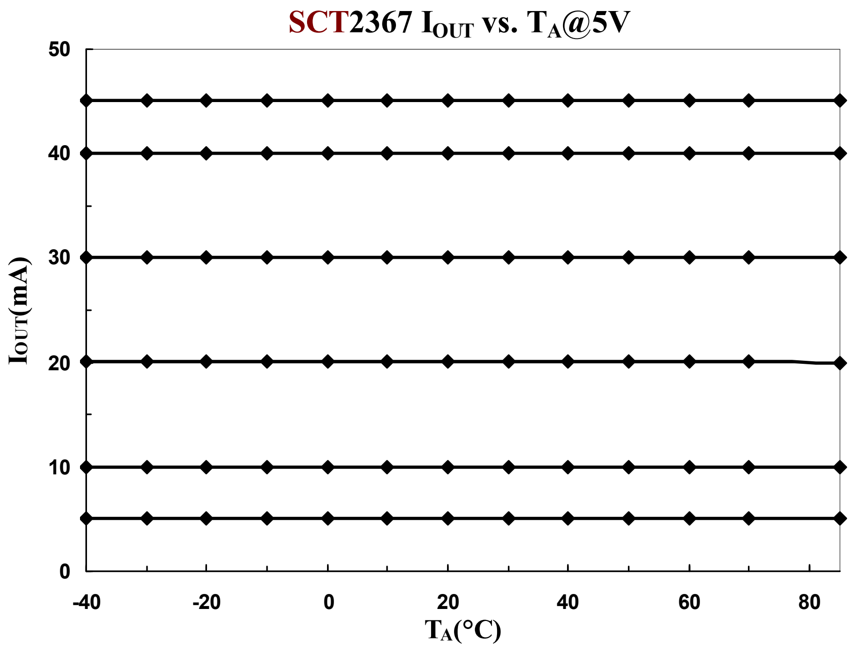
The current characteristic of output curve is flat. The output current can be kept constant regardless of the variations of LED forward voltage when $V_{OUT} > V_{DO}$(Drop-Out voltage). The relationship between I_{OUT} and V_{OUT} is shown below. The output voltage should be kept as low as possible to prevent the SCT2367 from being overheated.





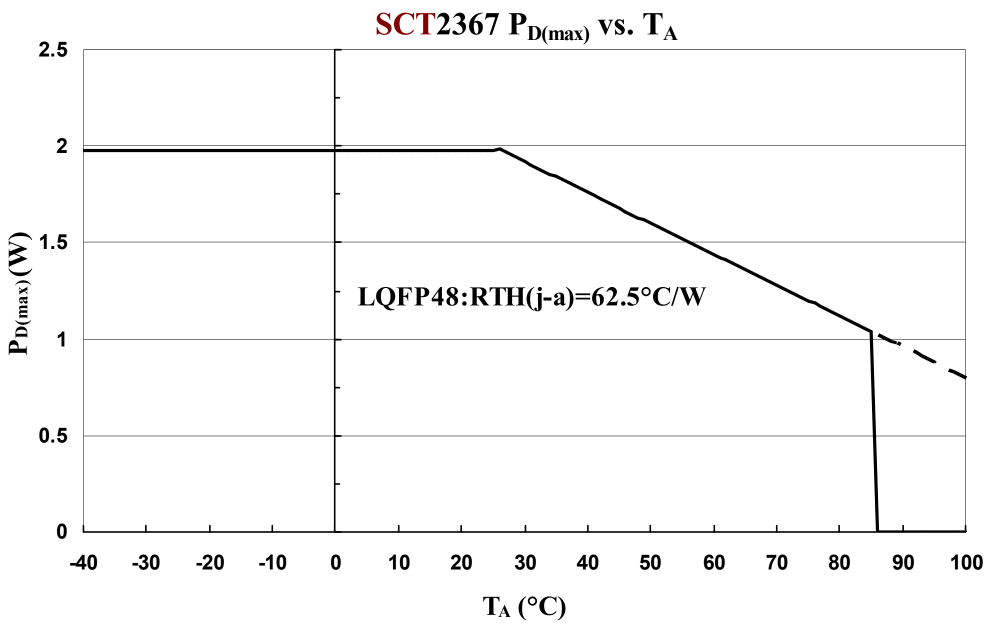
Excellent Temperature Regulation

The constant current driver requires not only the characteristics of supply and load voltage independence, but also temperature invariance. A well thermal stable reference circuit is designed within the SCT2367. Users can get the stable output current over recommended current range I_{OUT}=5mA~45mA with ambient temperature (T_A) widely varying from -40°C to 85°C.



Power Dissipation

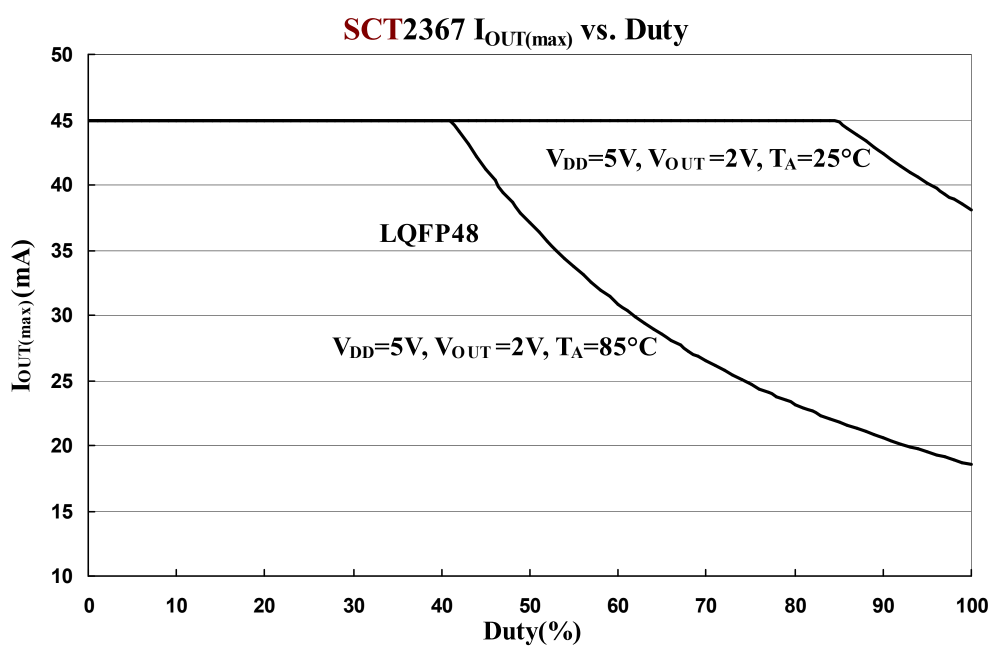
The maximum power dissipation ($P_{D(max)}$) of a semiconductor chip varies with different packages and ambient temperature. It's determined as $P_{D(max)}=(T_{J(max)} - T_A)/R_{TH(j-a)}$ where $T_{J(max)}$: maximum chip junction temperature is usually considered as 150°C, T_A: ambient temperature, $R_{TH(j-a)}$: thermal resistance. Since P=IV, for sinking larger I_{OUT}, users had better add proper voltage reducers on outputs to reduce the heat generated from the SCT2367.



Limitation on Maximum Output Current

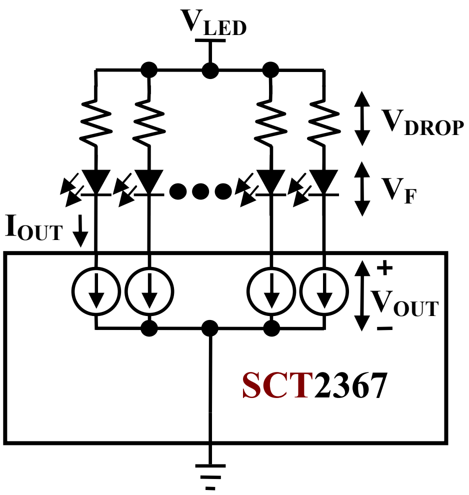
The maximum output current vs. duty cycle is estimated by:

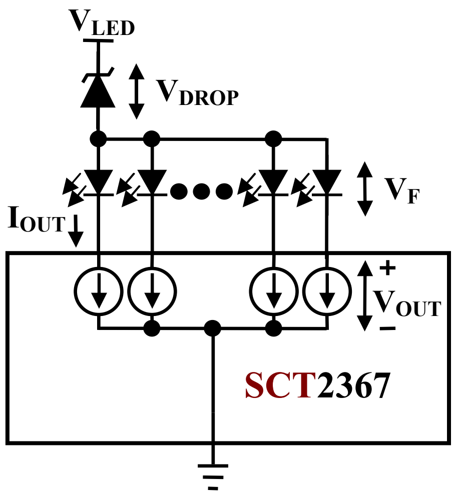
$I_{OUT(max)}=(((T_{J(max)}-T_A)/R_{TH(j-a)})-(3*V_{DD}*I_{DD}))/V_{OUT}/Duty/N$ where $T_{J(max)}$=150°C, N=24(all ON)



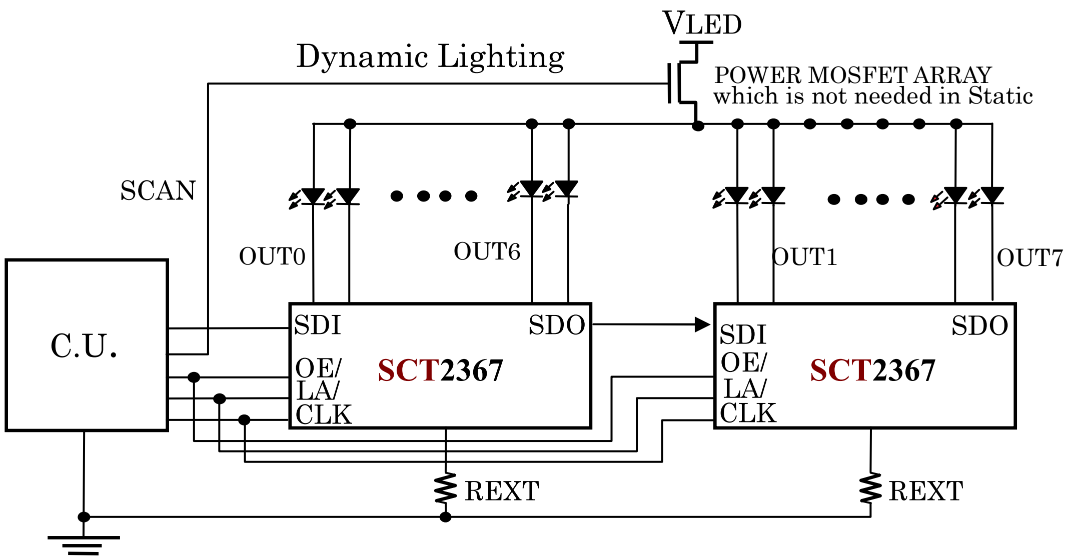
Load Supply Voltage (VLED)

The SCT2367 can be operated very well when V_{OUT} ranges from 1V to 4V. However, it is recommended to use the lowest possible supply voltage or set a voltage reducer to reduce the V_{OUT} voltage, at the same time reduce the power dissipation of the SCT2367. Suggested V_{OUT} is to be set greater than V_{DO} and less than 1V. The V_{DO} is dependent on the I_{OUT} current as indicated in section “Output Characteristics”. Follow the diagram instructions shown below to lower down the output voltage. This can be done by adding additional resistor or zener diode, thus $V_{OUT}=V_{LED}-V_{DROP}-V_F$.





Typical Application

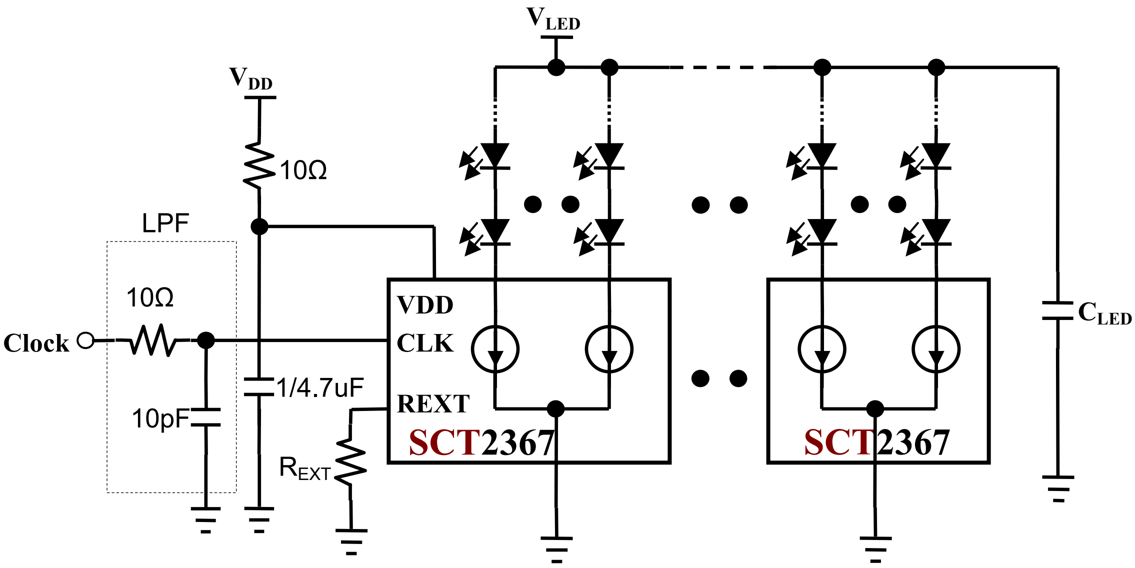


PCB Design Considerations

Use the following general guide-line when designing printed circuit boards **(**PCB**):**

Decoupling Capacitor

Place a decoupling capacitor e.g. 1uF between VDD and GND pins of SCT2367. Locate the capacitor as close to the SCT2367 as possible. This is normally adequate for static LED driving. For dynamic scan or PWM applications, it is necessary to add an additional capacitor of 4.7uF or more to each supply VDD_A, VDD_B, VDD_C for every SCT2367. The necessary capacitance depends on the LED load current, PWM switching frequency, and serial-in data speed. Inadequate VDD decoupling can cause timing problems, and very noisy LED supplies can affect LED current regulation.



External Resistor (R_{EXT})

Locate the external resistor as close to the REXT pin as possible to avoid the noise influence.

Power and Ground

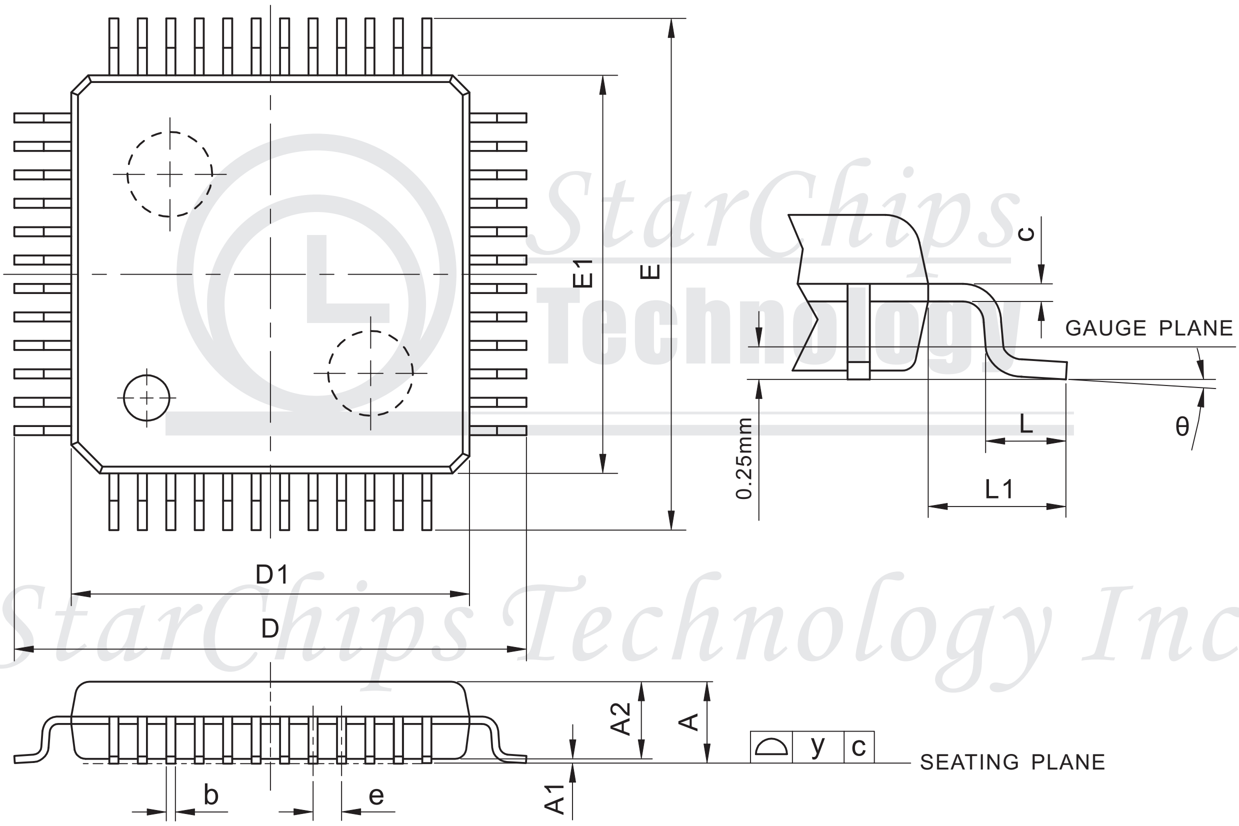
Maximizing the width and minimizing the length of VDD and GND trace improves efficiency and ground bouncing by effect of reducing both power and ground parasitic resistance and inductance. A small value of resistor, e.g., 10Ω (higher if I_{OUT} is larger) series in power input of the SCT2367 in conjunction with decoupling capacitor shunting the IC is recommended. Separating and feeding the LED power from another stable supply terminal V_{LED}, furthermore adding a capacitor C_{LED} greater than 10uF beside the LED are recommended. Please adapt C_{LED} according to total system current consumption.

EMI Reduction

To reduce the EMI radiation from system, an economical solution of RC low pass filter (LPF) is suggested to be used to lower the transient edge of clock input signal, as shown in the figure above. Using at least four layers PCB board with two interior power and ground planes is a good scheme to decrease the signal current path which is the source of radiation emission. As a result, EMI radiation can be decreased.

Package Dimension

LQFP48-7x7(check up-to-date version)



Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.60	-	-	63.0
A1	0.05	-	0.15	2.0	-	6.0
A2	1.35	1.40	1.45	53.0	55.0	57.0
b	0.17	0.22	0.27	6.7	8.7	10.6
c	0.178 TYP			7.0 TYP		
e	0.50 BSC			19.7 BSC		
D	8.90	9.00	9.10	350.0	354.0	358.0
D1	6.90	7.00	7.10	272.0	276.0	280.0
E	8.90	9.00	9.10	350.0	354.0	358.0
E1	6.90	7.00	7.10	272.0	276.0	280.0
L	0.50	0.60	0.70	20.0	24.0	28.0
L1	1.00 REF			39.0 REF		
y	-	-	0.10	-	-	3.9
θ	0°	3.5°	7.0°	0°	3.5°	7.0°

Revision History (check up-to-date version)

Data Sheet Version	Remark
V01_01	New Release

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