4-bit Serial-In/Parallel-Out PWM Constant Current Driver

Product Description

The SCT2007 is a 4-channel current-sink constant current driver incorporating patented PWM circuit. In general, three channels for typical RGB LEDs cluster and one additional channel for another red LED(2R1G1B) to enrich color saturation or lit up white LED(1R1G1B1W) to increase display or backlight brightness. In applications, users can set the output currents OUT[0:3] from 5mA to 90mA by one resistor for concurrent or four resistors for individual current setting. The serial data are shifted into shift register by clock rising edge. Input data appear at the DO output clock cycles later to allow cascading of multiple SCT2007s.

For the wire/line cost sensitive application, the SCT2007 provides two signal wires only (clock and data) to transmit serial data for long-distance cascaded operation. It also embeds clock and data buffers to regenerate input signals at the same time improve transmission quality for long-distance transmission. The SCT2007 embeds PWM gray scale controller to provide 10-bit gray scale and 12-bit global brightness for each output. Each output has 10-bit gray scale (1024 grayscales), thus three outputs represent 30-bit color. The minimum gray scale PWM pulse width ~80ns provides faster response time and more exquisite color presentation for RGB LED cluster application.

Since the high clock frequency can be reached up to 20MHz, the SCT2007 satisfies the system requirements of high volume data transmission to control the RGB LED for mix-color display. The higher clock frequency provides higher data transfer rate and faster refresh rate when many driver ICs connect in cascade configuration. Furthermore, the SCT2007 also provides TTL interface (supply independent input threshold), thus it can recognize the output signals issued from the controller system which is feed with power supply input less than typical 5V.

The excellent current regulation capability allows SCT2007 easily drive each output current to a constant stable output nearly without affected by power supply of LED, loading due to variant V_F of LEDs and operating temperature. The SCT007 is equipped with over temperature protection. The four channels IC stops driving the output while sense its junction temperature exceeds the 160°C high limit and the output will be reactivated while the junction temperature is below the 110°C low limit. In conclusion, the driver system is protected from damage of overheated.

Features

- Patent's two-wire only transmission SPI interface
- Inverting clock output to maximize timing budget for long-distance transmission
- 4 bit current-sink constant current driver for RGB and W clusters
- Current regulated output channels, constant current range: 5 – 90mA
- Enhanced 10x12-bit PWM color depth:

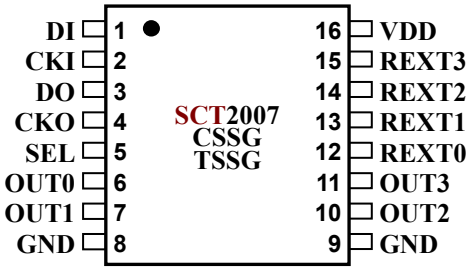
  10-bit grayscale control

  12-bit global brightness control (4096-step dot correction)
- Minimum gray scale PWM pulse width ~80ns
- Automatic data latched without complex input signals combination
- User adaptive frame refresh rate control
- Clock-synchronization PWM duty control
- The output current adjusted with corresponding external reference resistors
- Reference current allow to be set individually or concurrently
- ±2% current matching between outputs
- ±4% current matching between ICs
- Excellent regulation to load, supply voltage

  Load regulation: ±0.1%/V

  Line regulation: ±0.5%/V
- Excellent temperature compensation
- Embedded buffers to regenerate signals for cascade operation
- Over temperature protection
- Power on reset(POR) built-in to clear all outputs after power on
- Input interface 5V/3V (SCT2007C/T) discrete input options
- The maximum output sustain voltage: 17V
- PC platform base control system available
- DMX 512 controller commands set interpreter available
- Supply voltage: 5V
- Package: SSOP16
- Applications: Building decorative lighting, mesh display, LED strip, leisure lighting, Neon lamp

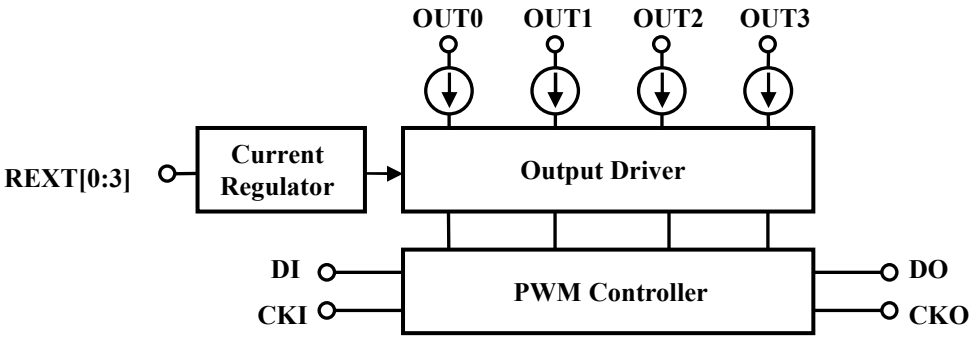
Pin Configurations



Terminal Description

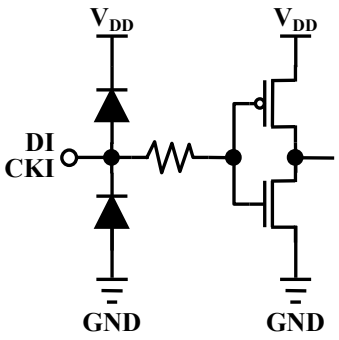
Pin No.	Pin Name	I/O	Function
1	DI	I	Serial data Input terminal
2	CKI	I	Clock input terminal of PWM controller
3	DO	O	Serial data output terminal
4	CKO	O	Output terminal of inverted CKI
5	SEL	I	SEL='0' all output current are commonly set by REXT0 terminal. SEL='1' select REXT0、REXT1、REXT2 and REXT3 to be the current setting terminals for OUT0、OUT1、OUT2 and OUT3 respectively
6,7,10,11	OUT[0:3]	O	Output terminal provide four constant current sinks
12-15	REXT[0:3]	I/O	Combining with SEL pin these pins used to connect external resistors from REXT0、REXT1、REXT2 and REXT3 to ground for setting up output current of OUT[0:3]
8	GND	-	Ground terminal for supply VDD pin
9	GND	-	Ground terminal for output OUT[0:3] pins
16	VDD	-	Supply voltage terminals

Block Diagram

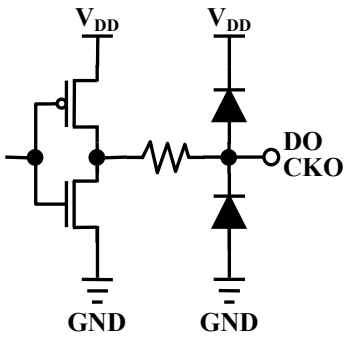


SCT2007

Equivalent Circuits of Inputs



Equivalent Circuits of Output



Ordering Information

Part	Marking	Package	Unit per reel(pcs)
SCT2007CSSG	SCT2007CSSG	Green SSOP16	2500
SCT2007TSSG	SCT2027TSSG		

StarChips Technology, Inc.

4F, No.5, Technology Rd., Science-Based Industrial Park, Hsin-Chu, Taiwan, R.O.C.

Tel : +886-3-577-5767 Ext.555

Fax: +886-3-577-6575

E-mail : service@starchips.com.tw

Maximum Ratings (T_A = 25°C)

Characteristic		Symbol	Rating	Unit
Supply voltage		V_{DD}	7.0	V
Input voltage		V_{IN}	-0.2 to V_{DD}+0.2	V
Output current		I_{OUT}	90	mA/Channel
Output voltage		V_{OUT}	-0.2 to 17	V
Total GND terminal current		I_{GND}	360	mA
Power dissipation	SSOP16	P_D	1.08	W
Thermal resistance	SSOP16	$R_{TH(j-a)}$	116	°C /W
Operating temperature		T_{OPR}	-40 to +85	°C
Storage temperature		T_{STG}	-55 to +150	°C

The absolute maximum ratings are a set of ratings not to be exceeded. Stresses beyond those listed under "Maximum Ratings" may cause the device breakdown, deterioration even permanent damage. Exposure to the maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (T_A= -40 to 85°C unless otherwise noted)

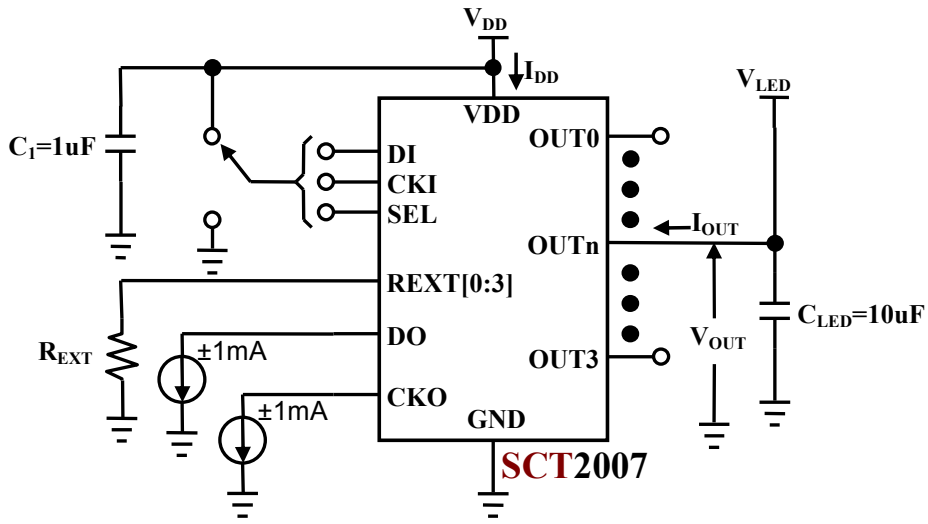
Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	-	4.5	5.0	5.5	V
Output voltage	V_{OUT}	Output ON	-	1	4	V
		Output OFF	-	-	17	V
Output current	I_{OUT}	DC test circuit	5	-	90	mA
Input voltage (SCT2007C)	V_{IH}	Input signals	0.7V_{DD}	-	V_{DD}+0.1	V
	V_{IL}	Input signals	-0.1	-	0.3V_{DD}	V
Input voltage (SCT2007T)	V_{IH}	Input signals	2	-	V_{DD}+0.1	V
	V_{IL}	Input signals	-0.1	-	0.4	V
Clock frequency	$f_{W(CKI)}$	-	-	-	20	MHz
Clock pulse width	$t_{W(CKI)}$	-	20	-	-	ns
Setup time	$t_{S(DI)}$	-	5	-	-	ns
Hold time	$t_{H(DI)}$	-	10	-	-	ns

Electrical Characteristics (T_A=25°C, V_{DD}=5V unless otherwise noted)

Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage (SCT2007C)		V_{IH}	-	0.7V_{DD}	-	V_{DD}	V
		V_{IL}	-	0	-	0.3V_{DD}	V
Input voltage (SCT2007T)		V_{IH}	-	2	-	V_{DD}	V
		V_{IL}	-	0	-	0.4	V
Output voltage		V_{OH}	V_{DD}=5V, I_{OH}= -1mA	V_{DD}-0.4	-	-	V
		V_{OL}	V_{DD}=5V, I_{OL}=+1mA	-	-	0.4	V
Output leakage current		I_{OL}	V_{OUT}=17V	-	-	0.5	uA
Output current		I_{OUT}	V_{OUT}=1V, R_{EXT}=900Ω	-	21	-	mA
Current bit skew[1]		dI_{OUT1}	V_{OUT}=1V, R_{EXT}=900Ω	-	±2	±3	%
Chip skew[2]		dI_{OUT2}	V_{OUT}=1V, R_{EXT}=900Ω		±4	±6	%
Line regulation[3] I_{OUT} vs. V_{DD}		%/dV_{DD}	4.5V<V_{DD}<5.5V, V_{OUT}>1V, R_{EXT}=900Ω	-	±0.5	±1	%/V
Load regulation[4] I_{OUT} vs. V_{OUT}		%/dV_{OUT}	1V<V_{OUT}<4V, I_{OUT}=21mA, V_{DD}=5V	-	±0.1	±0.5	%/V
Thermal shutdown		T_H	Junction temperature	-	160	-	°C
		T_L		-	110	-	°C
Supply current	OFF	$I_{DD(OFF)1}$	V_{DD}=5V, R_{EXT}=Open, SEL=0/1,OUT[0:3]=OFF	-	4/6	8	mA
		$I_{DD(OFF)2}$	V_{DD}=5V, R_{EXT}=900Ω, SEL=0/1,OUT[0:3]=OFF	-	6/18	10/20	
	ON	$I_{DD(ON)}$	V_{DD}=5V, R_{EXT}=900Ω, SEL=0/1,OUT[0:3]=ON	-	6/18	10/20	

1. Bit skew=(I_{OUT}-I_{AVG})/I_{AVG}, where I_{AVG}=($I_{OUT(max)}$+ $I_{OUT(min)}$)/2
2. Chip skew=(I_{AVG}-I_{CEN})/I_{CEN}*100(%), where I_{CEN} is the statistics distribution center of output currents.
3. Line regulation=[I_{OUT}(V_{DD}=5.5V)-I_{OUT}(V_{DD}=3V)]/(5.5V-3V)*100(%/V)
4. Load regulation=[I_{OUT}(V_{OUT}=4V)-I_{OUT}(V_{OUT}=1V)]/(4V-1V)*100(%/V)

Test Circuit for Electrical Characteristics

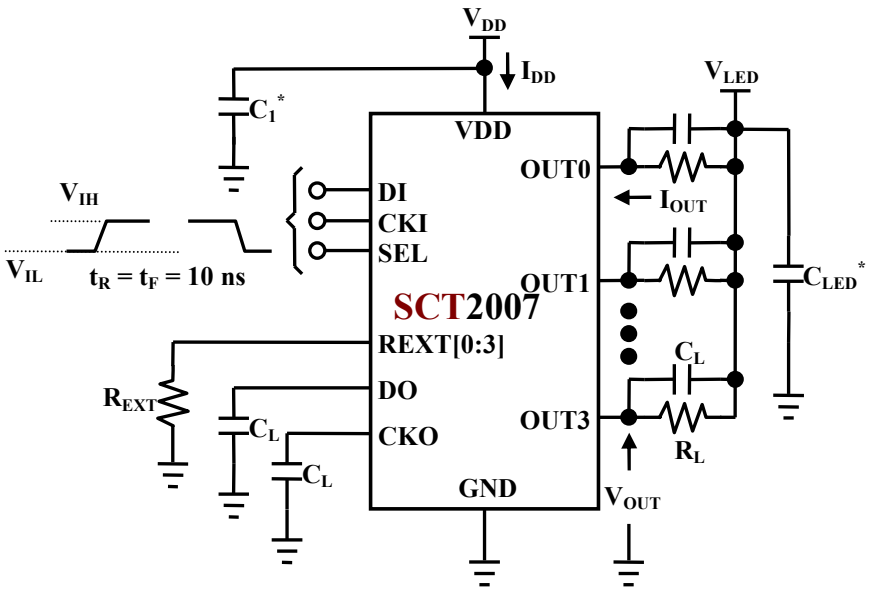


Switching Characteristics (T_A=25°C unless otherwise noted)

Characteristic		Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time ("L" to "H")	CKI - CKO	t_{PLH1}	V_{DD} = 5V V_{LED} = 5V V_{IH} = V_{DD} V_{IL}= GND SEL=0/1 R_{EXT} = 900Ω R_L = 180Ω C_L = 10pF C_1 = 1uF C_{LED} = 100uF	-	10	20	ns
	CKI - DO	t_{PLH2}		-	10	20	ns
	CKI - OUTn	t_{PLH3}		-	20	30	ns
Propagation delay time ("H" to "L")	CKI - CKO	t_{PHL1}		-	10	20	ns
	CKI - DO	t_{PHL2}		-	10	20	ns
	CKI - OUTn	t_{PHL3}		-	20	30	ns
Pulse width	CKI	$t_{W(CLK)}$		20	-	-	ns
	OUTn	t_W		120	-	-	ns
CKO/DO rise time	CKO	t_{R1}		-	5	10	ns
	DO	t_{R2}		-	5	10	ns
CKO/DO fall time	CKO	t_{F1}		-	5	10	ns
	DO	t_{F2}		-	5	10	ns
Setup time for DI		$t_{S(DI)}$		5	-	-	ns
Hold time for DI		$t_{H(DI)}$		10	-	-	ns
Output rise time of I_{OUT}		t_{OR}		-	20	30	ns
Output fall time of I_{OUT}		t_{OF}		-	20	30	ns
Slow CKI rise time[1]		t_R	Cascade	-	-	500	ns
Slow CKI fall time		t_F		-	-	500	ns

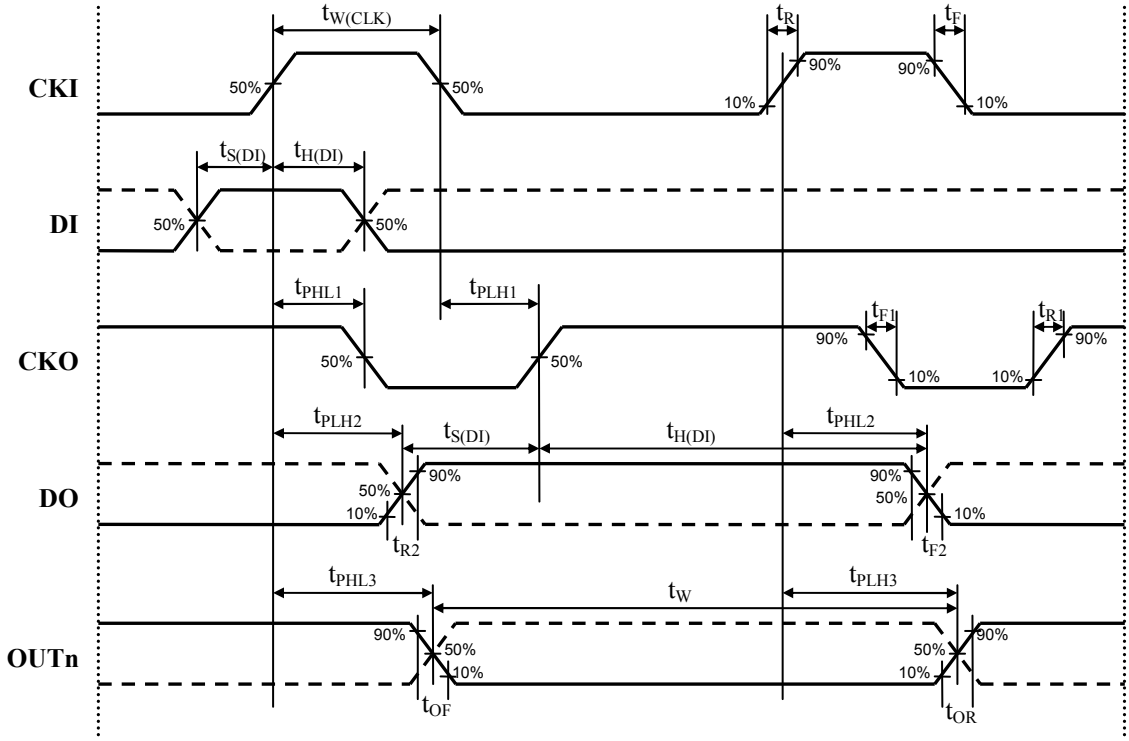
1. It may not be possible to achieve the timing requirment for data transfer if t_R and t_F is too large during cascaded operation.

Test Circuit for Switching Characteristics



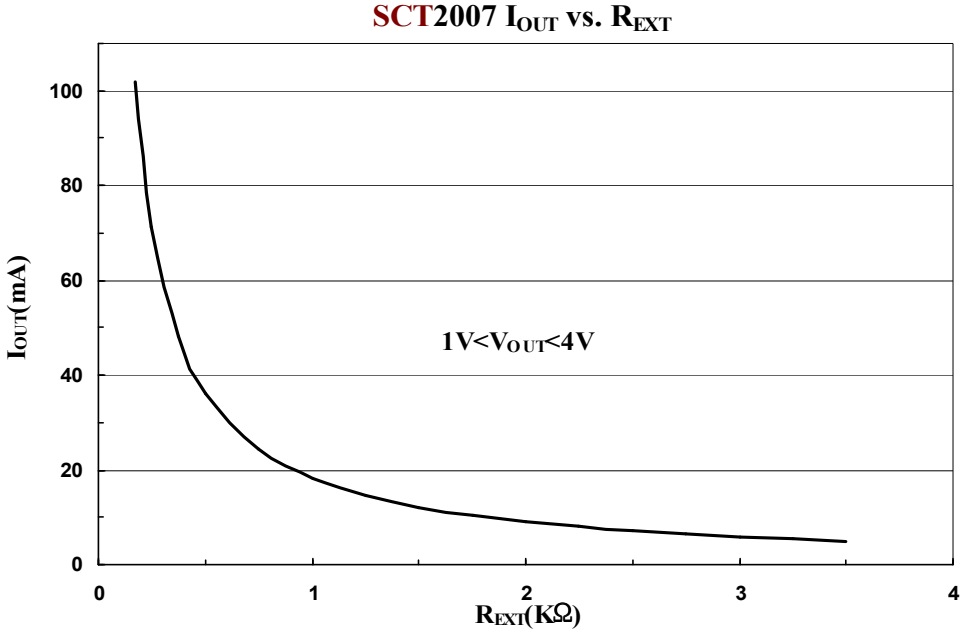
Place C_1/C_{LED} more close to IC VDD/OUT pin(not supply source) as possible.

Timing Waveform



Adjusting Output Current

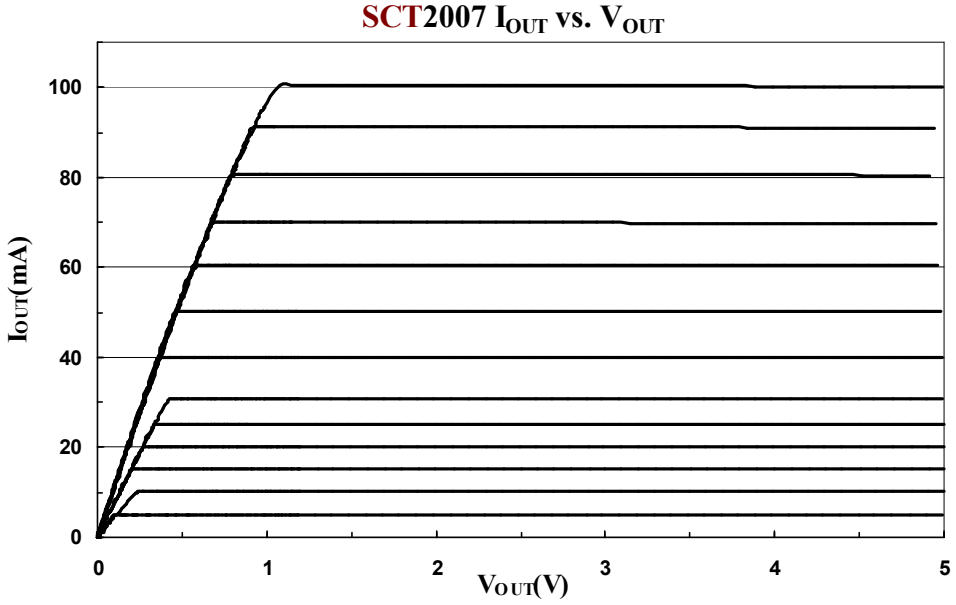
The SCT2007's output current (I_{OUT}) are set by external resistors at pins REXT[0:3]. The output current I_{OUT} versus resistance of R_{EXT} is shown as the following figure.



Furthermore, when SCT2007's output voltage is set between 1V and 4 V, the output current I_{OUT} can be estimated by the formula: I_{OUT} = 30(630 / R_{EXT}) (mA) (Chip skew < ±6%), Thus the output currents are set about 21mA at R_{EXT} = 900Ω.

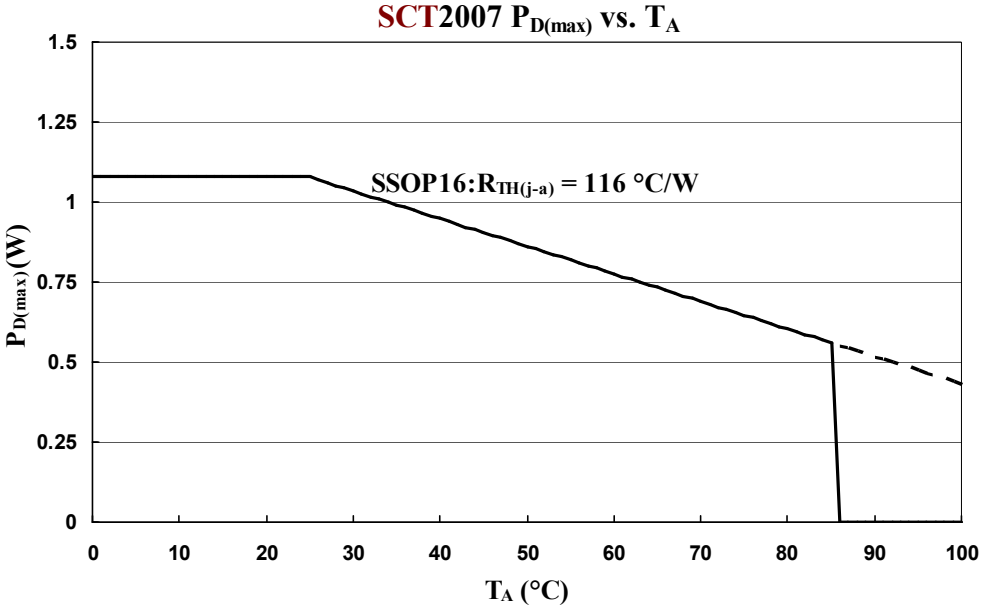
Output Characteristics

The current characteristic of output curve is flat. The output current can be kept constant regardless of the variations of LED forward voltage when V_{OUT} > 1V. The relationship between I_{OUT} and V_{OUT} is shown below.



Maximum Power Dissipation

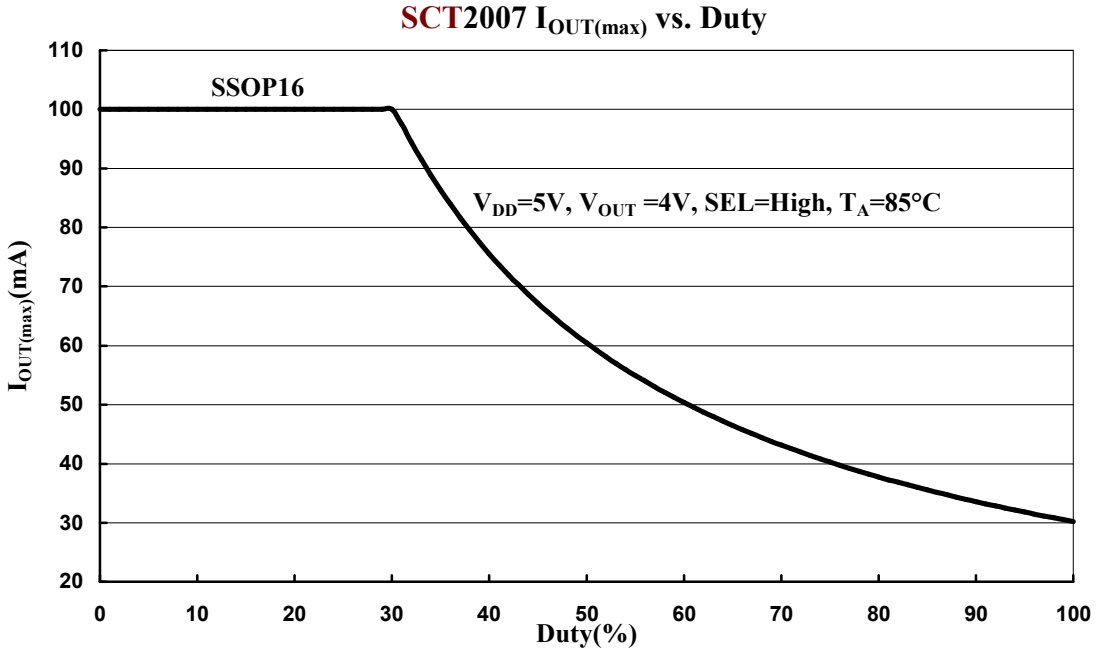
The maximum power dissipation ($P_{D(max)}$) of a semiconductor chip varies with different packages and ambient temperature. It's determined as $P_{D(max)}=(T_{J(max)} - T_A)/R_{TH(j-a)}$ where $T_{J(max)}$: maximum chip junction temperature is usually considered as 150°C, T_A: ambient temperature, $R_{TH(j-a)}$: thermal resistance. Since P=IV, for sink larger I_{OUT}, users had better add proper voltage reducers on output to reduce the heat generated from the SCT2007.



Limitation on Maximum Output Current

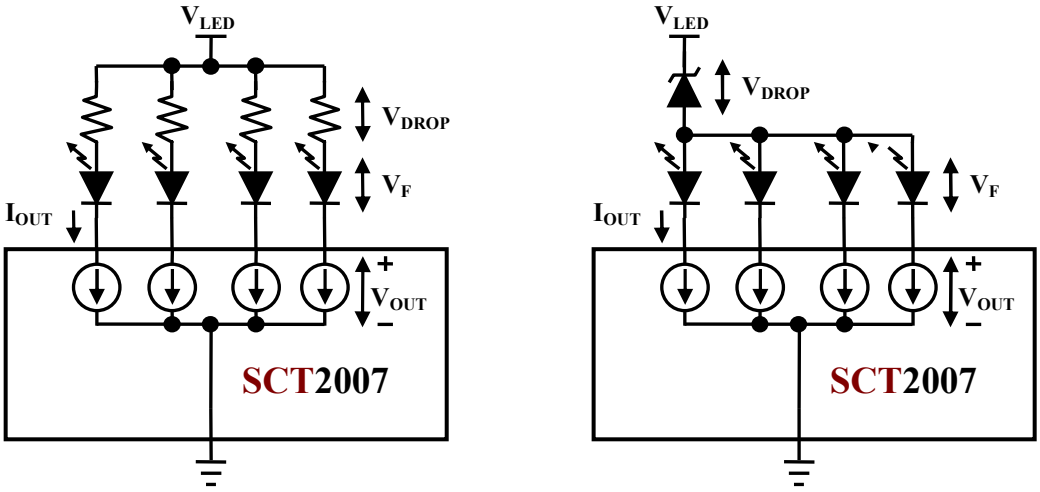
The maximum output current vs. duty cycle is estimated by:

$I_{OUT(max)}=(((T_{J(max)}-T_A)/R_{TH(j-a)})-(V_{DD}*I_{DD}))/V_{OUT}/Duty/N$ where $T_{J(max)}$=150°C, N=4(all ON)



Load Supply Voltage (VLED)

The SCT2007 can be operated very well when V_{OUT} ranges from 1V to 4V. It is recommended to use the lowest possible supply voltage or set a voltage reducer to reduce the V_{OUT} voltage, at the same time reduce the power dissipation of the SCT2007. This can prevent the IC from malfunction with thermal shutdown situation. Follow the diagram instructions shown below to lower down the output voltage. This can be done by adding additional resistor or zener diode, thus $V_{OUT}=V_{LED}-V_{DROP}-V_F$.



Over Temperature Shutdown

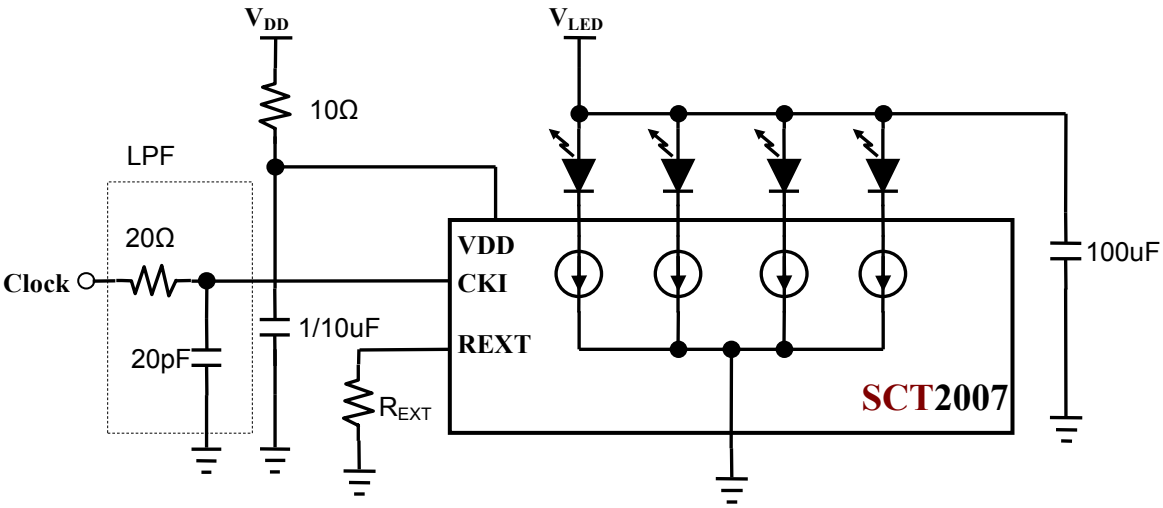
The SCT2007 contains thermal shutdown scheme to prevent damage from over heated. The internal thermal sensor turns off all outputs when the die temperature exceeds +160°C. The outputs are enabled again when the die temperature drops below +110°C. During the thermal shutdown process, the LEDs look blinking since it is turned OFF then ON periodically.

PCB Design Considerations

Use the following general guide-line when designing printed circuit boards (PCB):

Decoupling Capacitor

Place a decoupling capacitor e.g. 1uF between VDD and GND pins of SCT2007. Locate the capacitor as close to the SCT2007 as possible. This is normally adequate for static LED driving. For PWM applications, it is necessary to add an additional capacitor of 10uF or more to each supply for every SCT2007. The necessary capacitance depends on the LED load current, PWM switching frequency, and serial-in data speed. Inadequate VDD decoupling can cause timing problems, and very noisy LED supplies can affect LED current regulation.



External Resistor (REXT)

Locate the external resistor as close to the REXT pin as possible to avoid the noise influence.

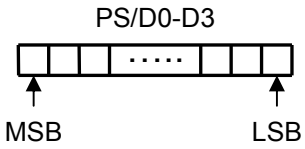
Power and Ground

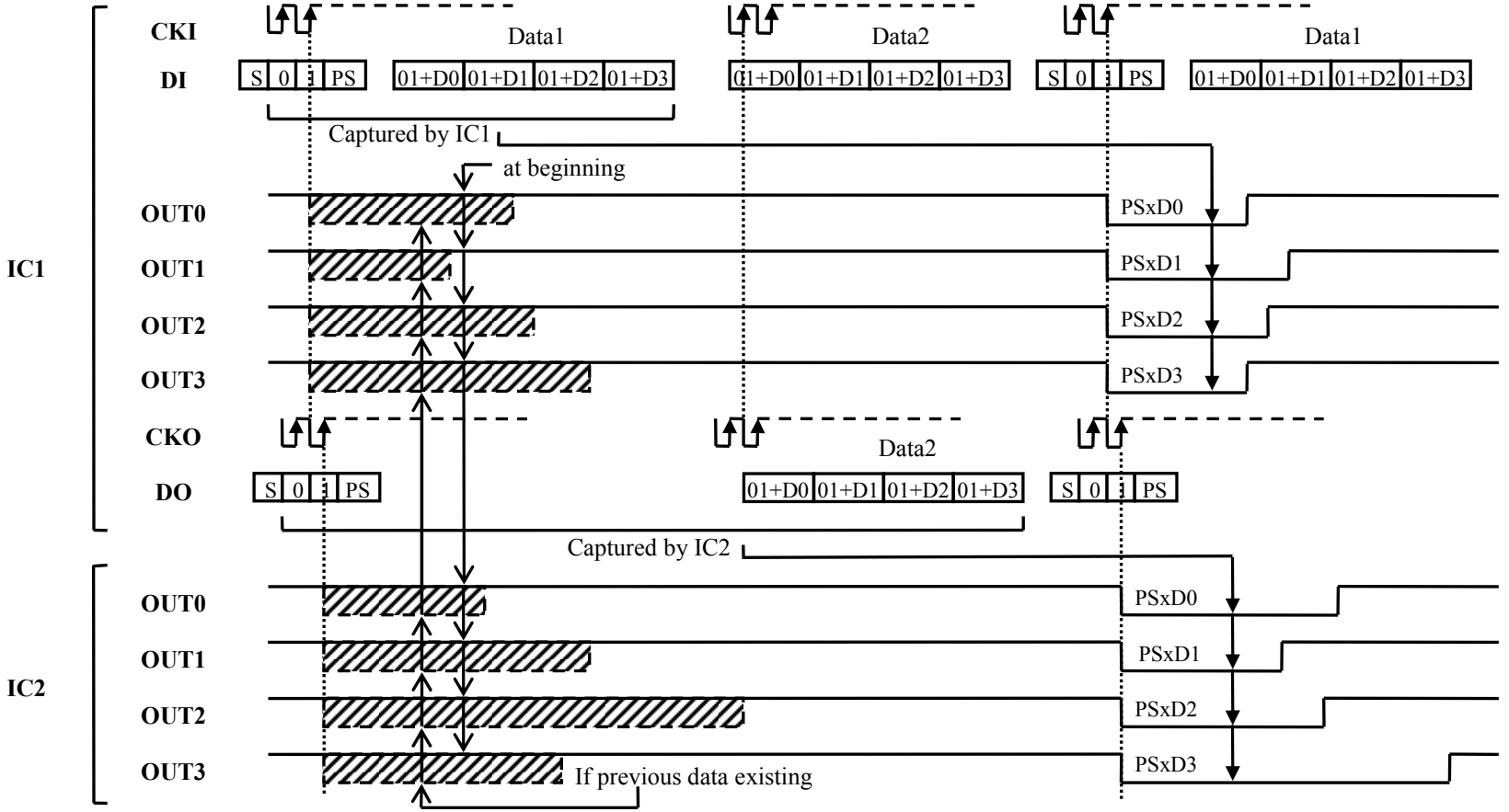
Maximizing the width and minimizing the length of VDD and GND trace improves efficiency and ground bouncing by effect of reducing both power and ground parasitic resistance and inductance. A small value of resistor e.g. 10Ω series in power input of the SCT2007 in conjunction with decoupling capacitor shunting the IC is recommended. Separating and feeding the LED power from another stable supply terminal V_{LED}, furthermore adding a larger capacitor e.g. 100uF beside the LED are strongly recommended.

EMI Reduction

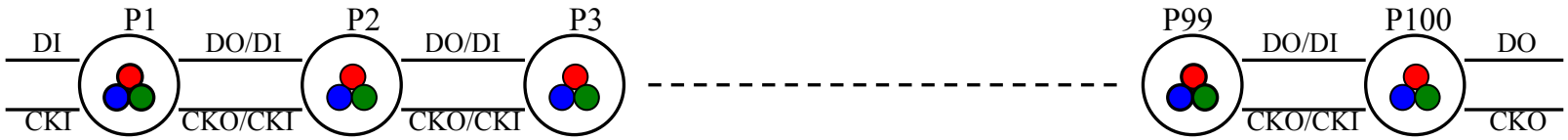
To reduce the EMI radiation from system, an economic solution RC low pass filter (LPF) is suggested to be used to lower the transient edge of clock input signal, as shown in the figure above. Using at least four layers PCB board with two interior power and ground planes is a good scheme to decrease the signal current path which is the source of radiation emission. As a result, EMI radiation can be decreased.

SCT2007 Timing Diagram and Data format

Input Data	Description
S(Start):16bits 1 PS(PreScalar):12bits D0-D3(Data):10bits 12*4=48 bits for each data 	1. data triggered at positive edge of clock input 2. “01” as data leading bits of PS/D0-D3 3. D0-D3 transmitted 48bits data in series 4. S/PS seen by all cascaded IC, also transmitted 30 bits in series 5. Valid input range for PS:1-4095, D0-D3:0-1023 6. CKO is inverted of CKI. 7. Data output at next start bit(exactly said, CKI rising edge of PS leading bit 1) 8. The prepared data should not less than the cascade driver ICs. 9. Add two or more tailing bits(00) at ending of frame data. 10. CKO/DO of IC1 cascaded to CKI/DI of IC2, Data1 captured by IC1, Data2 by IC2….



SCT2007 Application Example

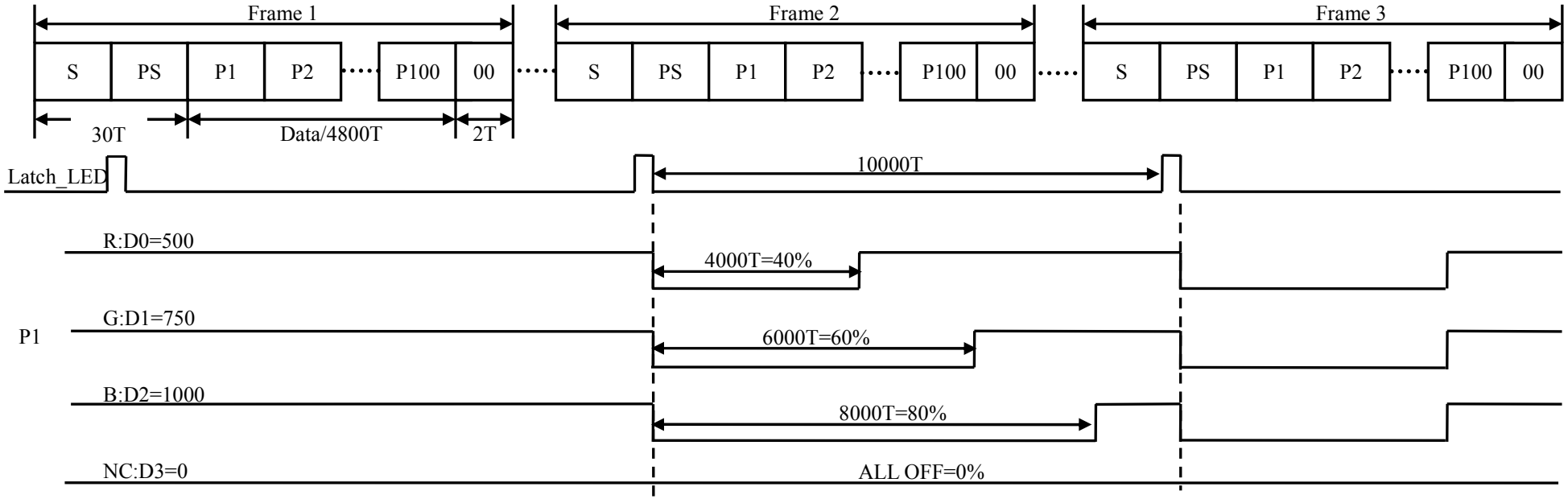


100 pixels for each LED series, each pixel consists of RGB(or 4) LEDs, the shown color is determined by modulated duty of each RGB LED.

Input clock CKI frequency = 1M, period = 1us, if system refresh rate is set to 100 Hz, i.e. period=10000uS=10000T, 1T=1uS.

Configuration: OUT0→R, OUT1→G, OUT2→B, OUT3→ NC , pulse width for each RGB: TR=PS*D0, TG=PS*D1, TB=PS*D2, Tx=PS*D3.

Data preparation ~ 48*100 = 4800T, 48T for each data, assume PS=8 which is usually as system-wise global brightness control.



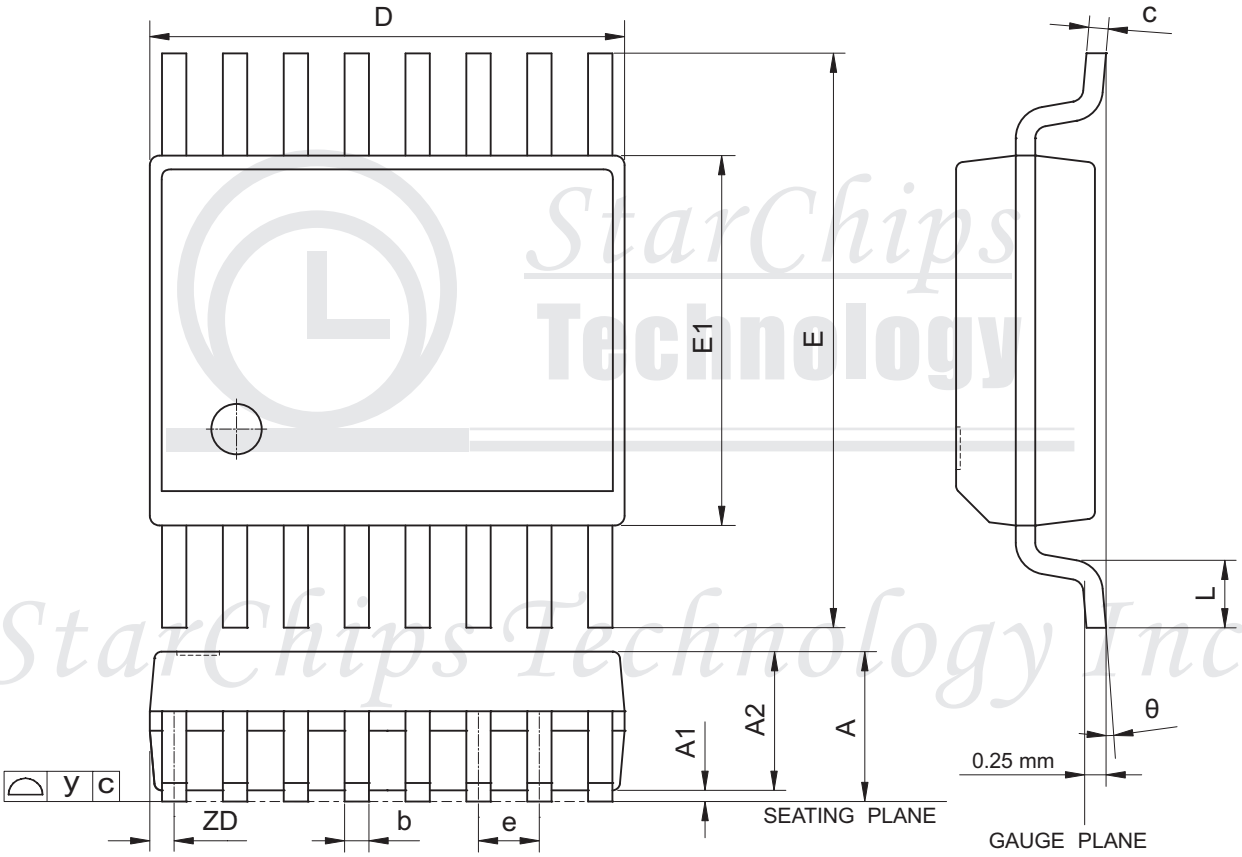
Note: Refresh rate is determined by S interval. The latched data is output at next internal Latch_LED falling edge, which is generated after S.

Maximum refresh rate ~ CKI/(30+48*pixels+2), add two tailing bits “0” at ending of each data frame. In this case, after last data P100, before next frame start bits S.

Maximum PS ~ CKI/(1023*refresh rate). In this case, 206 and 9 for maximum refresh rate and PS.

Package Dimension

SSOP16(check up-to-date version)



Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.35	1.63	1.75	53.1	64.2	68.9
A1	0.10	0.15	0.25	3.9	5.9	9.8
A2	-	-	1.50	-	-	59.1
b	0.20	-	0.30	7.9	-	11.8
c	0.18	-	0.25	7.1	-	9.8
D	4.80	4.90	5.00	189.0	192.9	196.9
E	5.79	5.99	6.20	228.0	235.8	244.1
E1	3.81	3.91	3.99	150.0	153.9	157.1
e		0.64 BSC			25.0 BSC	
L	0.41	0.64	1.27	16.1	25.0	50.0
y	-	-	0.10	-	-	3.9
ZD		0.23 REF			9.0 REF	
θ	0°	-	8°	0°	-	8°

Revision History (check up-to-date version)

Data Sheet Version	Remark
V01_01	New release

Information provided by StarChips Technology is believed to be accurate and reliable. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Starchips can not assume responsibility and any problem raising out of the use of the circuits. Starchips reserves the right to change product specification without prior notice.